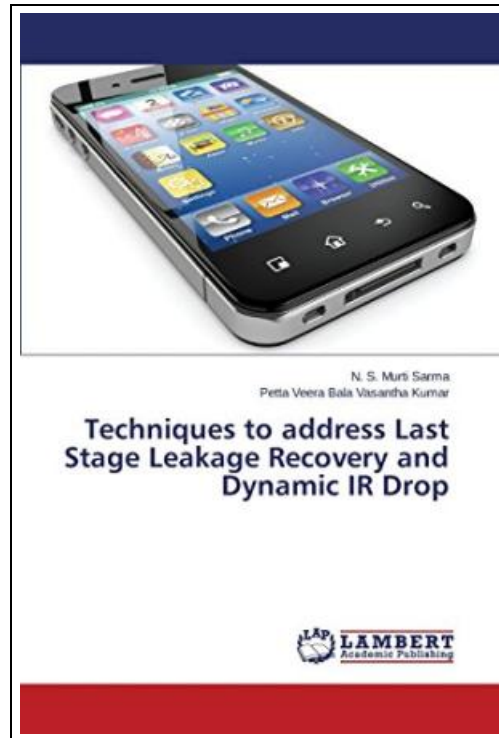


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TECHNIQUES TO ADDRESS LAST STAGE LEAKAGE RECOVERY AND DYNAMIC IR DROP



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Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | The leakage power, power integrity challenges due to spare cells and peak IR drop respectively are addressed in this monograph. The scope of the solution proposed lies in the Physical design level near to design closure where optimization tools have tight resources to fix these challenges. However, there is a lot of scope for future work in other areas of low PM spectrum like at circuit level, architectural level, design level and software coding level. Majority of today's semiconductor designers are not moved to very recent techniques like gate array ECO flows using ECO kits provided by library vendors due to efforts involved in modifying existing flows and tight design schedules. The proposed "Optimal State Assignment" technique can help reducing spare cells leakage without affecting design flows but switching to these new techniques will help in complete leakage power reduction of spare cells. Another possible area for future investigation is to use 65nm, 45nm, 32nm and 28nm libraries for various data flow intensive architectures implementation to validate the proposed "Selective Glitch Reduction" technique. | Format: Paperback | Language/Sprache: english | 116 pp.



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