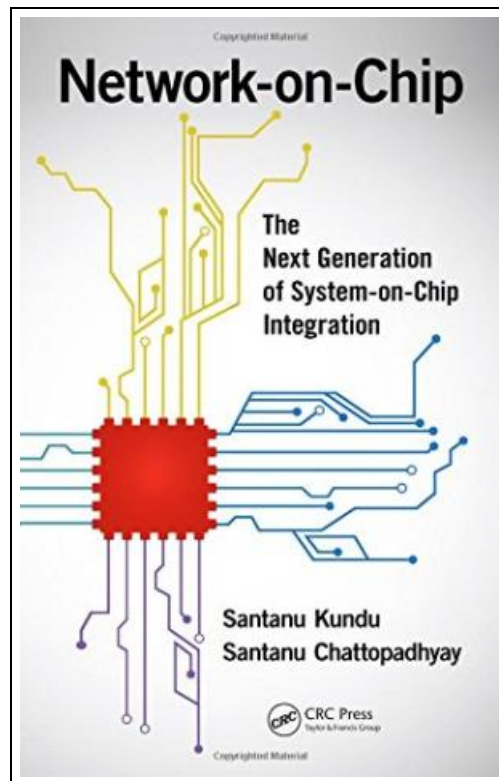# Network-On-Chip: The Next Generation of System-on-Chip Integration (Hardback)

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Taylor Francis Inc, United States, 2014. Hardback. Book Condition: New. 241 x 162 mm. Language: English . Brand New Book. Addresses the Challenges Associated with System-on-Chip Integration Network-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design, communication methodology, evaluation framework, and mapping of applications onto NoC. It details the design and evaluation of different proposed NoC structures, low-power techniques, signal integrity and reliability issues, application mapping, testing, and future trends. Utilizing examples of chips that have been implemented in industry and academia, this text presents the full architectural design of components verified through implementation in industrial CAD tools. It describes NoC research and developments, incorporates theoretical proofs strengthening the analysis procedures, and includes algorithms used in NoC design and synthesis. In addition, it considers other upcoming NoC issues, such as low-power NoC design, signal integrity issues, NoC testing, reconfiguration, synthesis, and 3-D NoC design. This text comprises 12 chapters and covers: * The evolution of NoC from SoC-its research and developmental challenges * NoC protocols, elaborating flow control, available network topologies, routing mechanisms, fault tolerance, quality-of-service support, and the design of network interfaces * The router design strategies followed in NoCs * The evaluation mechanism of NoC architectures * The application mapping strategies followed in NoCs * Low-power design techniques specifically followed in NoCs * The signal integrity and reliability issues of NoC * The details of NoC testing strategies reported so far * The problem of synthesizing application-specific NoCs *...

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